

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Richard E. Fackenthal	§	Group Art Unit:
		§	
Serial No.:		§	
		§	Examiner:
		§	
Filed:	October 16, 2003	§	
		§	
For:	Error Correction For Multi-Level Cell	§	Atty. Dkt. No.: ITL.1046US
	Memory With Overwrite Capability	§	(P17448)

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

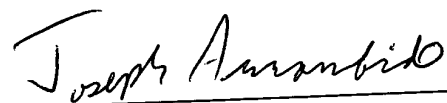
Dear Sir:

Applicant submits the references listed on the attached form PTO 1449 together with any required copies of patents, publications or other information of which applicant is aware, which applicant believes may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 C.F.R. § 1.56.

This statement is being filed with the application. Please apply any charges or credits to Deposit Account No. 20-1504 (ITL.1046US).

Respectfully submitted,

Date: October 16, 2003



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INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

ATTY DOCKET NO.
ITL.1046US (P17448)

SERIAL NO.

APPLICANT(S):
RICHARD E. FACKENTHAL

FILING DATE:
October 16, 2003

GROUP ART UNIT:

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A.	6,549,457	04/15/2003	SRINIVASAN ET AL.	365	185.03	
	B.	US2003/0053333	03/20/2003	RUDELIC ET AL.	365	185.03	
	C.						
	D.						
	E.						
	F.						
	G.						
	H.						
	I.						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	J.							
	K.							
	L.							
	M.							
	N.							
	O.							
	P.							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Q.	Construction of Polyvalent Error Control Codes for Multilevel Memories; Stefano Gregori, Pietro Ferrari, Rino Micheloni and Guido Torelli; pp. 751-754; 2000
	R.	An Error Control Code Scheme for Multilevel Flash Memories; Stefano Gregori, Osama Khouri, Rino Micheloni and Guido Torelli; pp. 45-49; 2001
	S.	Using Non-Volatile Memories for Disk Caching; John I. Garney; U.S. Patent Application Serial No.: 10/287,115; filed: November 4, 2002
	T.	
	U.	
	V.	
	W.	

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.